EAST Search History

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	347	438/106-107.ccls or 438/109.ccls.	US-PGPUB	OR	ON	2006/09/20 21:08
L2	15	1 and ((die wafer chip component IC (integrated adj circuit)) with impedance)	US-PGPUB	OR	ON	2006/09/20 21:09
L3	6	2 and ((interposer spacer interconnect$4 support reinforc$4) with package)	US-PGPUB	OR	ON	2006/09/20 21:09
L4	3	@ad <= "20031031" and 3	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2006/09/20 21:09
L5	3789	257/723-724.ccls. or 257/678.ccls. or 257/686.ccls. or 257/737-738.ccls. or 257/774.ccls.	US-PGPUB	OR	ON	2006/09/20 21:10
L6	168	5 and ((die wafer chip component IC (integrated adj circuit)) with impedance)	US-PGPUB	OR	ON	2006/09/20 21:15
L7	63	6 and ((interposer spacer interconnect$4 support reinforc$4) with package)	US-PGPUB	OR	ON	2006/09/20 21:15
L8	63	7 and ((interposer spacer interconnect$4 support reinforc$4) and package)	US-PGPUB	OR	ON	2006/09/20 21:10
L9	30	8 and ((impedance resistance) with (PCB board substrate))	US-PGPUB	OR	ON	2006/09/20 21:15
L10	15	@ad <= "20031031" and 9	US-PGPUB	OR	OFF	2006/09/20 21:15
L11	1793	361/803-804.ccls. or 361/784.ccls. or 361/780.ccls. or 361/790.ccls. or 361/794.ccls.	USPAT	OR	ON	2006/09/20 21:20
L12	156	11 and ((die wafer chip component IC (integrated adj circuit)) with impedance)	USPAT	OR	ON	2006/09/20 21:20
L13	43	12 and ((interposer spacer interconnect$4 support reinforc$4) with package)	USPAT	OR	ON	2006/09/20 21:20
L14	26	13 and ((impedance resistance) with (PCB board substrate))	USPAT	OR	ON	2006/09/20 21:15
L15	26	@ad <= "20031031" and 14	USPAT	OR	OFF	2006/09/20 21:20
L16	253	361/803-804.ccls. or 361/784.ccls. or 361/780.ccls. or 361/790.ccls. or 361/794.ccls.	US-PGPUB	OR	ON	2006/09/20 21:20

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L17	47	16 and ((die wafer chip component IC (integrated adj circuit)) with impedance)	US-PGPUB	OR	ON	2006/09/20 21:20
L18	11	17 and ((interposer spacer interconnect$4 support reinforc$4) with package)	US-PGPUB	OR	ON	2006/09/20 21:21
S1	250590	(die wafer chip component IC (integrated adj circuit)) with (impedance resistance)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/09/20 19:42
S2	560616	(die wafer chip component IC (integrated adj circuit)) with (interposer spacer interconnect$4 support reinforc$4)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/09/20 17:52
S3	56188	(interposer spacer interconnect$4 support reinforc$4) with package	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/09/20 19:43
S4	175350	(impedance resistance) with (PCB board substrate)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/09/20 19:43
S5	1465	S1 and S2 and S3 and S4	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2006/09/20 17:53
S6	1162	@ad <= "20031031" and S5	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2006/09/20 19:44
S7	1	10/698,906	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2006/09/20 17:57

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S8	1	S7 and signal	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/09/20 17:58
S9	823	S6 and signal	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/09/20 17:59
S10	207	S9 and (signal adj path)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/09/20 19:40
S11	7340	257/723-724.ccls. or 257/678.ccls. or 257/686.ccls. or 257/737-738.ccls. or 257/774.ccls.	USPAT	OR	ON	2006/09/20 21:10
S12	414	S11 and ((die wafer chip component IC (integrated adj circuit)) with impedance)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/09/20 21:10
S13	145	S12 and ((interposer spacer interconnect$4 support reinforc$4) with package)	USPAT	OR	ON	2006/09/20 21:10
S14	270	S12 and ((interposer spacer interconnect$4 support reinforc$4) and package)	USPAT	OR	ON	2006/09/20 21:10
S15	155	S14 and ((impedance resistance) with (PCB board substrate))	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/09/20 21:10
S16	142	@ad <= "20031031" and S15	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2006/09/20 20:00

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S17	129	S16 not S10	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2006/09/20 19:59
S18	583	438/106-107.ccls or 438/109.ccls.	USPAT	OR	ON	2006/09/20 21:08
S19	33	S18 and ((die wafer chip component IC (integrated adj circuit)) with impedance)	USPAT	OR	ON	2006/09/20 21:09
S20	13	S19 and ((interposer spacer interconnect$4 support reinforc$4) with package)	USPAT	OR	ON	2006/09/20 21:09
S21	13	@ad <= "20031031" and S20	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2006/09/20 21:11
S22	7	S21 and ((impedance resistance) with (PCB board substrate))	USPAT	OR	ON	2006/09/20 21:08